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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Narumi OHKAWA**

Serial No.: **NEW**

Filed: **April 8, 1999**

For: **SEMICONDUCTOR DEVICE HAVING BOTH MEMORY AND LOGIC CIRCUIT AND ITS MANUFACTURE**

CLAIM FOR PRIORITY UNDER 35 U.S.C. 119

Assistant Commissioner for Patents
Washington, D. C. 20231

Date: April 8, 1999

Sir:

The benefit of the filing date of the following prior foreign application is hereby requested for the above-identified application, and the priority provided in 35 U.S.C. 119 is hereby claimed:

Japanese Appln. No. 10-281699, Filed October 2, 1998

In support of this claim, the requisite certified copy of said original foreign application is filed herewith.

It is requested that the file of this application be marked to indicate that the applicant has complied with the requirements of 35 U.S.C. 119 and that the Patent and Trademark Office kindly acknowledge receipt of said document.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON

William F. Westerman
Attorney for Applicant
Reg. No. 29,988

Atty. Docket No. **990355**
1725 K Street, N.W., Suite 1000
Washington, DC 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
WFW/llf

日 本 国 特 許 庁
PATENT OFFICE
JAPANESE GOVERNMENT

別紙添付の書類に記載されている事項は下記の出願書類に記載されてる事項と同一であることを証明する。
This is to certify that the annexed is a true copy of the following application as filed h this Office.

出 願 年 月 日
ate of Application: １９９８年１０月 ２日

出 願 番 号
plication Number: 平成１０年特許願第２８１６９９号

願 人
licant (s): 富士通株式会社

１９９９年 ２月１９日

特 許 庁 長 官
Commissioner,
Patent Office 伊佐山建志

出証番号 出証特平１１－３００８０４